REMARKS

Claims 2, 6, and 8-13 have been examined. Claims 2, 8, 9 and 10 have been amended. Claims 2, 6, and 8-13 remain. Applicant respectfully requests reconsideration of this application.

Rejections under 35 U.S.C. §102(e)

The Examiner has rejected claims 2, 6, 8, and 11 under 35 U.S.C. §102(e) as being anticipated by Maruyama. Applicant respectfully traverses this rejection. Applicant respectfully submits that Maruyama does not teach or suggest that potential faults are identified for testing by backtracing from each observable node through logic gates *and* memory elements. In addition, Applicant respectfully submits that Maruyama does not teach or suggest that this backtracing *is limited* to paths along which a faulty value has a *possibility* of propagating to an observable node. Applicant respectfully submits that the reason for this difference between Maruyama and the present claims is best understood with the following example.

In the example used herein, there is a logic circuit network containing a logical AND gate having two inputs (A and B) and one output (C). Inputs A and B are fed from logic that can be stimulated by either a tester, the chip input pins (i.e., the primary inputs) or by scannable latches. Output C feeds logic that can be measured at the tester, chip output pins or scannable latches.

In Maruyama, the logic circuit network is analyzed starting from points measured by a tester, which is a hardware device that makes electrical connection with the pins on the device. Maruyama describes performing good machine simulation and finding an "activation path" from a "circuit branch point" to another "circuit branch point". Maruyama, Col. 13, lines 14-24. These "circuit branch points" include stimulation points on the input side and measure

points on the output side. As those having ordinary skill in the art would recognize, an "activation path" as described in Maruyama is a path that allows both a 1 and a 0 from a first point to a second point. Thus, if Maruyama performs good machine simulation that results in a 0 on both input pins A and B of the AND gate of the logic circuit network, then there is no "activation path" through that AND gate even though there may be an activation path from the output pin C of the AND gate to a measure point. This is because any single fault that may cause a 1 in a fault machine at pin A will not produce a 1 in the fault machine at pin C. The reason for this is that 0 on pin B (which is assumed to be a zero in the fault machine because it is assumed that no single defect will affect BOTH pins A and B) will block the 1 on input pin A from reaching output pin C. The same argument holds for a fault that feeds pin B. Therefore, Maruyama will identify an activation path from point C forward, and *not consider* any of the logic feeding pins A and B. Maruyama, Col. 12, lines 18-40.

Applicant respectfully submits that the manner in which the "activation paths" are used in Maruyama is different than the manner in which the present invention backtraces through logic blocks. First, Maruyama defines an activation path *between* circuit branch points, which ultimately end at either memory elements, circuit inputs or circuit outputs. Maruyama does not try to identify faults across memories in a single detection pass, which is another important distinction between Maruyama and the present claims. Maruyama, Col. 12, lines 31-40. [1] In contrast, the presently claimed invention does backtrace through memories.

[1] Note that if Maruyama were to backtrace through memory, the system disclosed therein would not be able to simulate the test patterns in parallel. This is because Maruyama depends on true-value simulation results in a single circuit state to perform parallel simulation of a multiplicity of patterns. The circuit state changes when a clock is pulsed.

Moreover, Maruyama defines every fault on an activation path as "detected". Maruyama, Col. 13, Lines 14-24 ("An undetected fault--which is present in the activation path--is set in the circuit information holding section 19 as being a detected fault."). The fact that Maruyama defines every fault as "detected" is an important distinction, as it means that the detection status of Maruyama only defines whether a good machine/fault machine difference *can* arrive at the receiving memory element. If the fault effect arrives at a receiving memory element, it is not yet marked as detected at a tester by Maruyama. Instead, the information about the fault that made it to that memory element is written to a storage element associated. Maruyama, Col. 12, lines 25-40. Maruyama describes the process of moving to the next circuit state when a clock pulse arrives. Maruyama, Col. 12, lines 25-40. This clock pulse enables the fault effect to be viewed on the output of the memory element. At this time, if there is an activation path starting at that memory element and going forward to a measure point, Maruyama marks the fault as detected by the tester. Maruyama *must* do this fault-writing, fault-reading, fault-passing process so that it can work on each circuit state in the test patterns independently (and therefore, can fault simulate patterns in parallel.)

In contrast to Maruyama, the claimed subject matter performs good machine simulation and then traces backwards in both the logic and in time, starting at each observable node. During this backtracing, the claimed invention traces through the combinational logic, memories and the various circuit states that make up the test to identify every fault that *could possibly* arrive at the measure point. The specification of the present application explicitly defines how to backtrace through each kind of logic block. See, for example, Figures 7-15 and the associated discussion at pages 14-21.

Thus, applying the presently claimed subject matter to the logic circuit network example described above, where there is a 0 on both pins A and B in the AND gate, the presently claimed invention will backtrace into, but not through (or behind) the AND gate. The reason for this is that the presently claimed subject matter is not trying to mark faults along the activation path as "detected" as in Maruyama. Rather, the presently claimed subject matter attempts to identify *which* faults the tester, given the good machine circuit state, *could* detect. In other words, the limitation present in every claim of the present application requiring that the backtracing be "limited to paths along which a faulty value has a possibility of propagating to said observable node" is not present in Maruyama.

Rejections Under 35 U.S.C. §103

The Examiner has rejected claims 9, 10, 12 and 13 under 35 U.S.C. §103(a) as being unpatentable over Maruyama in view of the alleged knowledge in the art. Applicant respectfully traverses this rejection. As discussed above, Maruyama does not teach or suggest backtracing through memories and does not teach or suggest that the backtracing be "limited to paths along which a faulty value has a possibility of propagating to said observable node". Because limitations in each of the claims are neither taught nor suggested by Maruyama, Maruyama cannot render claims 9, 10, 12 and 13 obvious.

Conclusion

In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would

be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (650) 614-7660. If there are any additional fees required, please charge Deposit Account No. 15-0665.

Respectfully submitted,

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